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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,217	POMAREDE ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed September 28, 2004.

Response to Amendment

The limitations added to claims 1 and 9 are sufficient to overcome the Moore reference. Therefore, the rejections of claims 1, 9, 10 and 15 as being anticipated by Moore (US 6,649,543), claims 2, 3 and 11 as being unpatentable over Moore in view of Ma et al. (US 6,297,539), claims 4-6 and 12-14 as being unpatentable over Moore in view of Ma et al. and Setton (US 6,727,148), and claims 7 and 8 as being unpatentable over Moore in view of Aoki et al. (US 6,744,104) are hereby withdrawn.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-3, 9-11 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Mahawili (US 6,800,830).

Regarding claim 1, Mahawili discloses forming a gate dielectric over a semiconductor substrate, exposing the gate dielectric to a source of nitrogen excited species, wherein exposing incorporates less than about 10% atomic nitrogen at a depth of greater than about 10 Angstroms from an upper surface of the gate dielectric and depositing a silicon-containing gate electrode over the gate dielectric after exposing the gate dielectric to the source of nitrogen excited species such that the gate electrode contacts a portion of the gate dielectric exposed to the source of nitrogen excited species (Fig. 8; col. 8, ln. 13-50).

Regarding claims 2 and 3, Mahawili discloses that the gate dielectric can include zirconium oxide or hafnium oxide (col. 10, ln. 1-7).

Regarding claim 9, Mahawili discloses forming an oxide layer over a semiconductor substrate, exposing an upper surface of the oxide layer to products of a plasma such that less than 10 atomic % of the products of the plasma are incorporated into the oxide layer at a depth of greater than 10 Angstroms from the upper surface and depositing a silicon-containing gate electrode over the upper surface after exposing the upper surface to the products of the plasma such that the gate electrode contacts the upper surface of the oxide layer (Fig. 8; col. 8, ln. 13-50).

Regarding claim 10, Mahawili discloses that the oxide layer serves as a gate dielectric.

Regarding claim 11, Mahawili discloses that the oxide layer may include zirconium oxide (col. 10, ln. 1-7).

Regarding claim 15, Mahawili discloses that the products of the plasma include nitrogen excited species.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahawili in view of Setton (US 6,727,148, previously cited).

Regarding claims 4 and 12, Mahawili does not disclose exposing the surface of the substrate to a source of nitrogen excited species prior to forming the gate dielectric. Like Mahawili, Setton discloses a method of making a gate oxide for a MOS transistor. Setton

teaches that when forming a metal oxide gate dielectric layer on a semiconductor substrate, there is a likelihood that the surface of the substrate will be oxidized, thus causing a problem of increasing high tunneling current through the dielectric. In order to avoid this problem, Setton exposes the surface of the substrate to a source of nitrogen excited species (plasma) prior to forming the gate dielectric to create an interfacial layer of silicon nitride on the substrate (col. 1, ln. 21-57; col. 3, ln. 6-27). The interfacial layer prevents high tunneling current. At the time of the invention, it would have been obvious to one of ordinary skill in the art to expose the substrate surface to nitrogen excited species prior to forming the gate dielectric of Mahawili because Setton teaches that by forming an interfacial layer between the substrate and the gate dielectric, high tunneling current through the gate dielectric can be prevented.

Regarding claims 5 and 13, Setton discloses that exposing the surface of the substrate to nitrogen excited species can form a silicon nitride layer on the surface of the substrate (thus, no silicon oxynitride is formed) (col. 3, ln. 6-27).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahawili in view of Setton, as applied to claims 5 above, and further in view of Ma et al. (US 6,297,539, previously cited).

Regarding claim 6, Mahawili discloses that the gate oxide can be a metal oxide but does not disclose how the metal oxide is deposited. Like Mahawili, Ma discloses a method of forming a metal oxide gate dielectric layer. Ma teaches that by using atomic layer deposition (ALD) to form the metal oxide gate dielectric layer, the gate dielectric layer can be created to be extremely uniform in thickness and composition (col. 3, ln. 11-34). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use atomic layer deposition to form the

metal oxide gate dielectric layer of Mahawili because Ma teaches that using ALD to form the metal oxide layer can form a gate dielectric that is very uniform in thickness and composition.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahawili in view of Aoki et al. (US 6,744,104, previously cited).

Regarding claim 7, Mahawili does not disclose that the silicon-containing gate electrode includes silicon-germanium. Like Mahawili, Aoki discloses a method of forming a MOS transistor. Aoki teaches that by forming a portion of the gate electrode of silicon-germanium by CVD, the transistor can be protected against leakage of a doped impurity into the channel region (col. 3, ln. 15-22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the silicon-containing gate electrode of Mahawili with a silicon-germanium gate, because Aoki teaches that a silicon-germanium gate offers the advantage of protecting the transistor against leakage of a doped impurity into the channel region.

Regarding claim 8, Aoki discloses that the silicon-germanium gate is formed by flowing germane (GeH_4) over the gate dielectric (col. 14, ln. 15-20).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahawili in view of Ma et al.

Regarding claim 14, Mahawili discloses that the gate oxide can be a metal oxide but does not disclose how the metal oxide is deposited. Like Mahawili, Ma discloses a method of forming a metal oxide gate dielectric layer. Ma teaches that by using atomic layer deposition (ALD) to form the metal oxide gate dielectric layer, the gate dielectric layer can be created to be extremely uniform in thickness and composition (col. 3, ln. 11-34). At the time of the invention, it would

have been obvious to one of ordinary skill in the art to use atomic layer deposition to form the metal oxide gate dielectric layer of Mahawili because Ma teaches that using ALD to form the metal oxide layer can form a gate dielectric that is very uniform in thickness and composition.

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
December 9, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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